TD 12.4 Ovonic Unified Memory - A High-performance Nonvolatile Memory Technology for Stand Alone Memory and Embedded Applications

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This paper discusses the development status of OUM (Ovonic Unified Memory), a phase-change, nonvolatile semiconductor memory technology for VLSI stand-alone memory and embedded applications. A 4 Mb VLSI test memory has been used as a development vehicle with 0.18um 3V CMOS. Characterization of the OUM technology is reviewed for high density, low voltage, high cycle-count nonvolatile memory applications with short programming times. OUM offers advantages in cell size, process complexity, cost, write times, cycling, cell energy consumption during write and direct over-write.

Data storage is accomplished in an OUM cell by a thermally induced phase change between amorphous and polycrystalline states in a thin film of chalcogenide alloy similar to the materials used in rewriteable CD and DVD optical disks. This rapid, reversible structural change in the $Ge_xSb_yTe_z$ alloy film results in a change in material resistivity that is measured during the read operation. OUM technology uses a short electrical pulse to achieve the amorphous state (high resistance RESET state) and lower but a bit longer current pulse to convert to the polycrystalline state (lower resistance SET state). The portion of the alloy film near a bottom resistive electrode changes state as a result of joule heating during the programming pulse [1]. Because of the small programmable volume of the film, the programming energy is small – suitable for portable communication applications.

Fig. 12.4.1 shows multiple oscilloscope traces of the cycling characteristics of the OUM memory cell element. Each trace is a series of 4 sequential operations, write/read/write-complement/read, cycling at 5MHz. An 8nS reset pulse is applied with a ~5nS falling edge. The subsequent read shows a programmed resistance of 85Kohms. Next application of a set pulse of 85nS results in a resistance of 2Kohms. The beginning of the set pulse shows the device threshold voltage, Vth, to be approximately 0.6V. The maximum device voltage required for memory operation occurs during the reset programming pulse, which is < 0.8V. The plot shows the superposition of 21 separate scope traces taken throughout 2E8 cycles at logarithmic time intervals.

At 0.18um lithography, a maximum device voltage of 0.8V and a diode voltage drop of 0.8-0.9V during the RESET operation allows 1.0V for CMOS control circuitry in a 3V CMOS operation. This avoids the high voltage transistors needed in Flash and other non-volatile memories under development. OUM memory is seamlessly embedded in a logic process by using low temperature OUM memory process modules after transistor formation.

Fig. 12.4.2 shows I-V characteristics of the chalcogenide memory element for both the SET and RESET states. When a voltage above Vth is applied to a device in the RESET state, the device switches electronically to a low resistance dynamic state, permitting low voltage programming. The figure also shows a significant separation between the read current and set/reset currents, allowing disturb-free read. Fig. 12.4.3 shows the read resistance of the cell as a consequence of the application of variable amplitude programming current pulses. Current programming pulses of incrementally increasing amplitude are applied with a read between each programming pulse. Data is shown both for a memory cell element initially in the SET and RESET states.

Memory array operation is shown in Fig. 12.4.4 indicating select and deselect conditions in the array. No discernable thermal disturb of adjacent bits has been observed, consistent with simulations. The non-addressed bit is fully deselected, so half select disturbs during write or write-complement are not a concern.

Fig. 12.4.5 shows the SET and RESET resistance of a single cell element cycled at 5 MHz. The OUM cell exhibits more than 10x dynamic range over more than 1E12 SET/RESET cycles, and, therefore, provides adequate sense margin.

Fig. 12.4.6 shows a photomicrograph of the 4 Mbit test chip used as a cell array development vehicle. Memory arrays with cell sizes ranging from $5F^2$ to $8F^2$ have been built using 0.18 um photolithography. The 4Mbit test chip is made up of eight 512Kbit planes. Each plane contains sixteen 32Kbit blocks, and each 32Kbit block of 128 rows by 256 columns is connected to each of 16 IO's. Each 512Kbit plane contains local sense amplifiers and a programming circuit, control circuit and X and Y decoders for independent operation. The X and Y decoder each have an enable signal (XEN and YEN) directly from a pad such that the tester can enable the X, Y or both decoders so as to control the sequence and timing of decode.

The Write operation timing is controlled by YEN. When YEN is "low," liobus (local IO bus line) is pre-charged to 2V to prevent any overshoot on the selected bit line at the YEN rising edge. Addresses are changed only while YEN is "low." The selected cell is written when YEN is "high." The selected WL is "gnd," and the selected bit line is connected to liobus and biased to 2V from the current source. All the unselected word lines are biased to "Vdd," and all the unselected bit lines are biased at "gnd." The current source is a simple PMOS current mirror, not a charge pump. Therefore, write operation requires only CMOS signals. Treset/Tset (YEN pulse width for resetting/setting the cell) are adjustable from 5ns to 200ns with Ireset/Iset (programming current for the cell) adjustable from 100uA to 1mA.

The Read operation timing also is controlled by YEN. When YEN is "low," liobus is pre-charged to VREF and sense amplifier is equalized for fast sensing. At YEN's rising edge, the precharge for liobus is disabled and liobus starts moving high/low from VREF depending on the cell data being read. The output from the 1st sense amplifier reach their steady state within 10ns, and the latch signal is activated to amplify the output from the 1st stage and load the newly sensed data to the data latch. YEN pulse width less than 12ns is observed for proper read operation. Fig 12.4.7 shows the simulated waveforms for Read operation including YEN, LATCH, OE and 2 output signals.

Eight sets of 8 option bits (CB<0:63>) are provided to reconfigure the test chip and to test the device in different conditions. For example, CB<0:7> controls the set and reset current as well as different sensing current, and CB<8:15> provides different timing control configuration including internal YEN pulse width control, XEN to YEN skew control.

Array cycling and reliability measurements as a function of ambient temperature such as programming characteristics vs. temperature, data retention, and array failure mechanisms are underway.

Acknowledgements
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References

[1] Stefan Lai and Tyler Lowrey, "OUM - A 180 nm Nonvolatile Memory Cell Element Technology For Stand Alone and Embedded Applications," IEDM 2001.

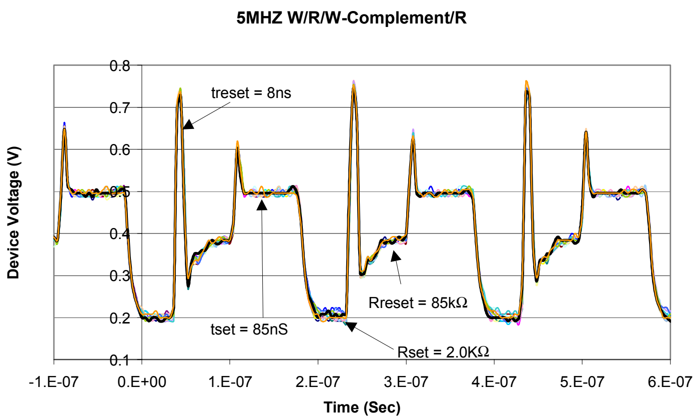


Fig 12.4.1 Oscilloscope traces of voltage drop across OUM cell during repetitive write/read/write-complement/read cycling.

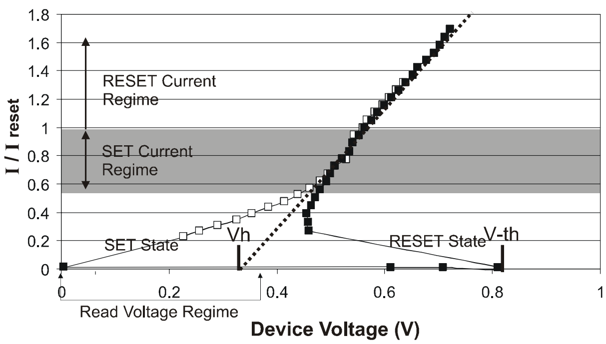


Fig. 12.4.2 Current – voltage characteristics for OUM cell element in both the RESET and SET state showing key device parameters: Read/SET/RESET regimes, SET and RESET states, Vh (holding voltage), and Vth (switching threshold voltage).

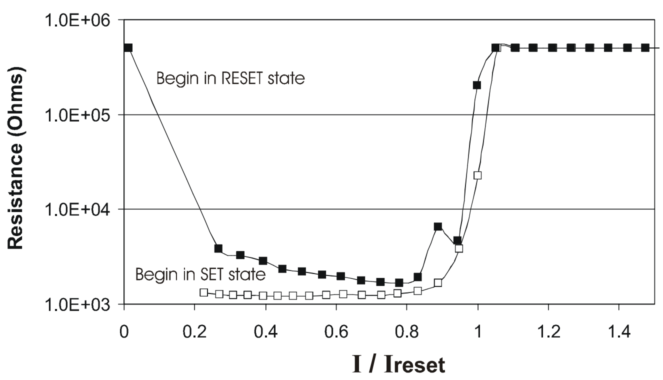
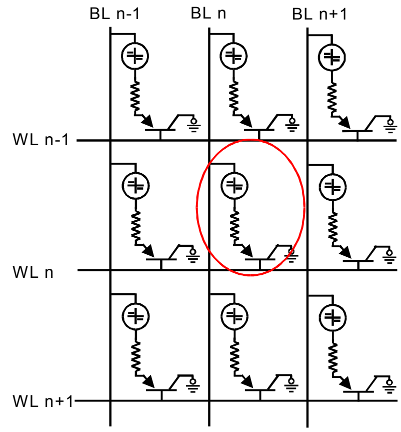


Fig. 12.4.3 Device resistance vs. applied programming current pulse.



	BL n-1	BL n	BL n+1	WL n-1	WL n	WL n+1
RESET	0 V	I_{RESET}	0 V	Vdd	0 V	Vdd
SET	0 V	I_{SET}	0 V	Vdd	0 V	Vdd
READ	0 V	I_{READ}	0 V	Vdd	0 V	Vdd

Fig. 12.4.4 Schematic diagram of memory array operation showing select and deselect conditions

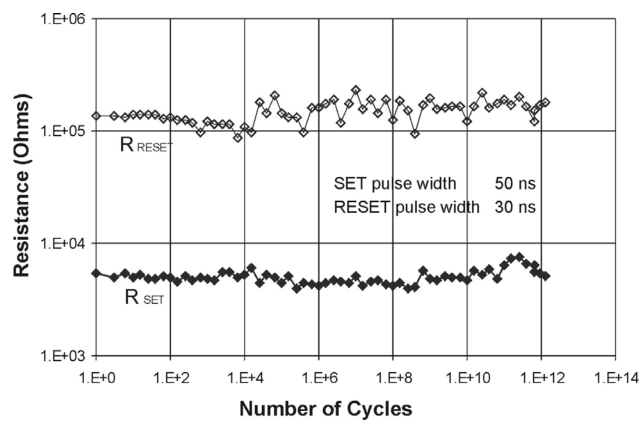


Fig. 12.4.5 SET and RESET resistance as a function of number of cycles of a single cell element.

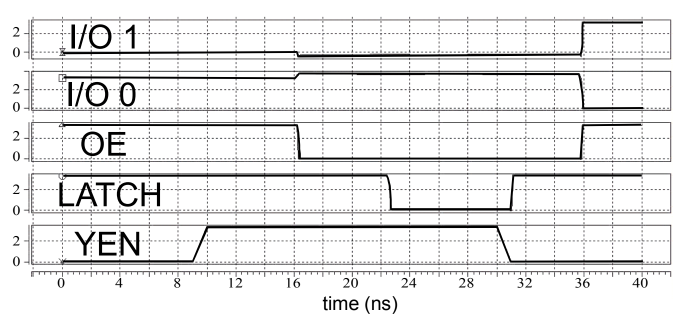


Fig. 12.4.7 Data path simulation.

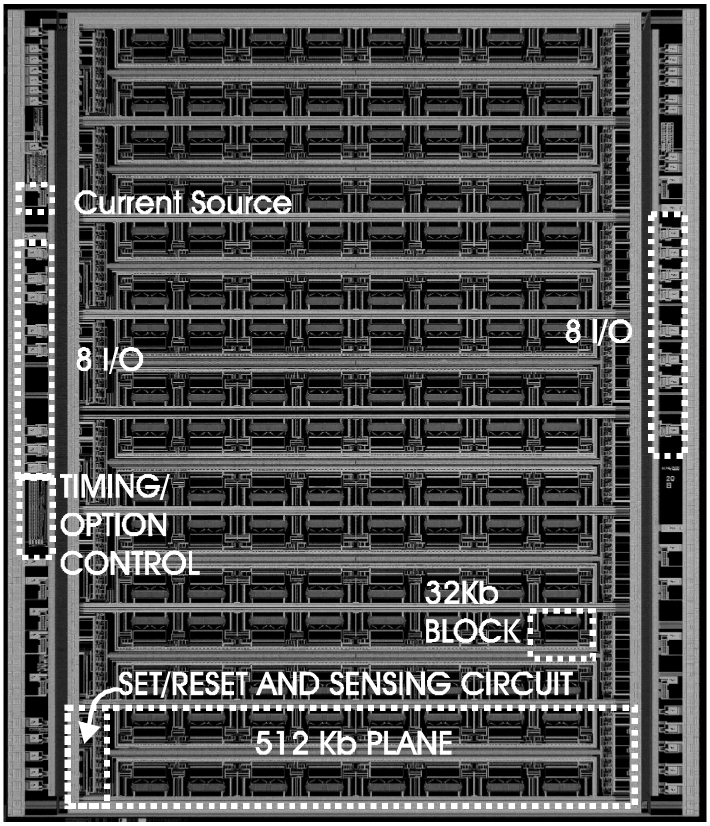


Fig. 12.4.6 Photomicrograph of 4 Mb test memory.

Figure Captions:

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